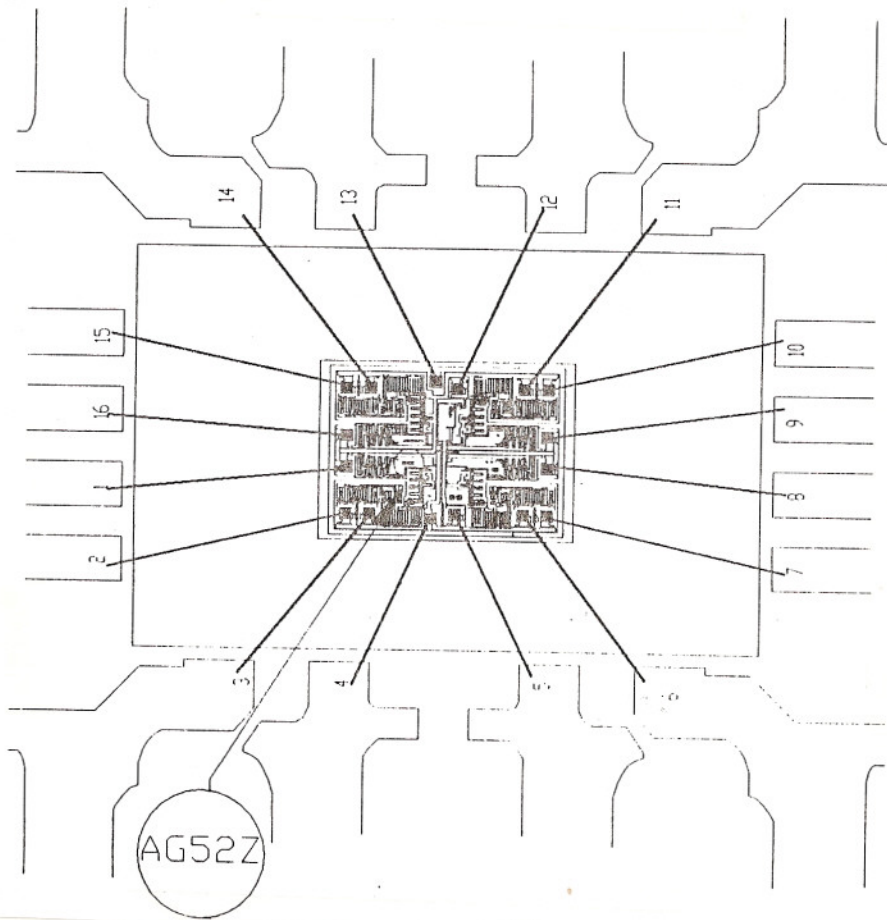




# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal: -**  
**Backside: -**  
**Backside Potential: -**  
**Mask Ref: -**  
**Bond Pads: .004"**

**APPROVED BY: CD**  
**MFG: Maxim**

**DIE SIZE: .072" x .102"**  
**THICKNESS: -**

**DATE: 7/1/02**  
**P/N: DG442**

DG 10.1.2  
Rev A 3-4-99